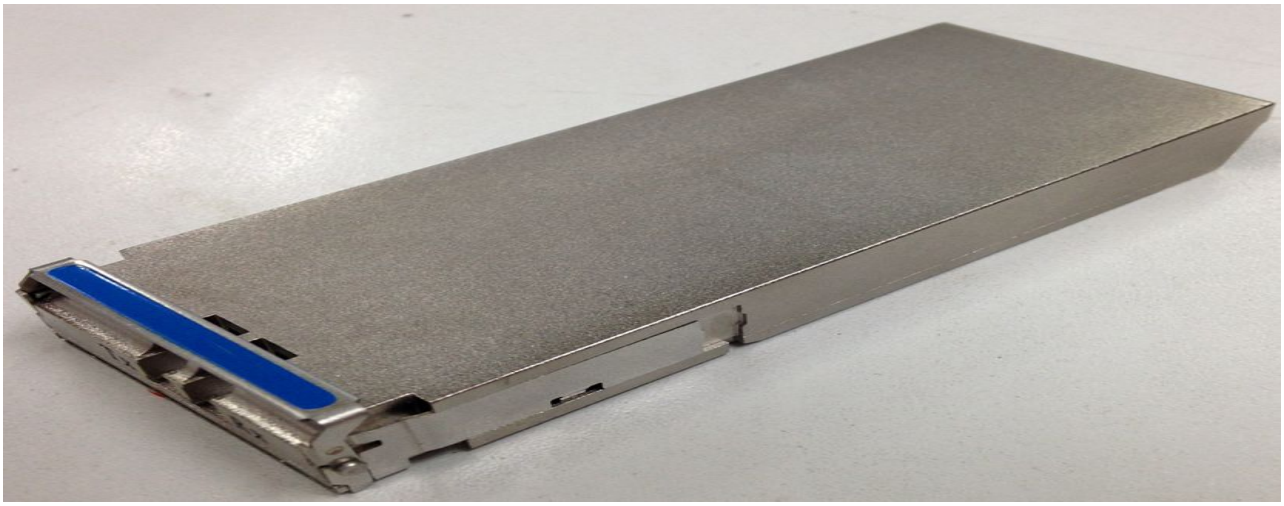


100Gb/s CFP2 Optical Transceiver

RTXM290-608

Features

- *Direct LC receptacle optical interface*
- *Single +3.3V power supply*
- *Hot-pluggable*
- *Operating optical data rate up to 112Gbps*
- *Transmission distance up to 40km*
- *AC coupling of CML signals*
- *1310 nm window cooled EA-DFB LD*
- *Integrated SOA、PIN ROSA and TOSA*
- *Low power dissipation(Max:9W)*
- *Built in digital diagnostic function*
- *Operating case temperature range:0℃ to 70℃*
- *Compliant with RoHs*
- *MDIO Communication Interface*

Application

- *Local and wide area network (LAN and WAN)*
- *Ethernet switches and router applications*
- *ITU-T OTU4 OTL4.4 applications*

Standards

- *Compliant with IEEE 802.3ba*
- *Compliant with CFP2 MSA hardware specification,Version1.0 July 31,2014*
- *Compliant with CFP MSA management specification，Version2.2July 01, 2013*
- *Compliant with ITU-T G.959.1*
- *Compliant with RoHS&WEEE*

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.5	+3.6
Operating Case Temperature Range	Tc	°C	-5	75
Receiver Damage Threshold Per Lane	P_{dag}	dBm	+5.5	

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	0		70
Power Supply Voltage	Vcc	V	3.2	3.3	3.4
Data rate		Gb/s		103.125	112

Specifications *(tested under recommended operating conditions, unless otherwise noted)*

Parameter		Symbol	Unit	Min	Typ	Max	Notes
Voltage Supply Electrical Characteristics							
Supply Current	Tx Section / Rx Section	Icc	A	-	-	2.75	1
Power Supply Noise		Vrip				2%	DC-1MHz
						3%	1-10MHz
Dissipation	Class3	Pw	W			9	
Low Power Dissipation		Plow	W			2	
Inrush Current	Class3	I-inrush	mA/usec			200	
Turn-off Current		I-turnoff	mA/usec	-200			
Different Signal Electrical Characteristics							
Single Ended Data Input Swing			mV	55	-	525	
Single Ended Data Output Swing			mV	150	-	500	
Differential Signal Output Resistance			Ω	80		120	
Differential Signal Input Resistance			Ω	80		120	
3.3V LVCMOS Electrical Characteristics							
Input High Voltage		3.3VIH	V	2.0	-	Vcc+0.3	
Input Low Voltage		3.3VIL	V	-0.3	-	0.8	
Input Leakage Current		3.3IIN	uA	-10	-	+10	
Output High Voltage (I_{OH}=100uA)		3.3VOH	V	Vcc-0.2	-	-	

Output Low Voltage (I_{OL}=100uA)	3.3VOL	V			0.2	
Minimum Pulse Width of Control Pin Signal	t_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics						
Input High Voltage	1.2VIH	V	0.84		1.5	
Input Low Voltage	1.2VIL	V	-0.3		0.36	
Input Leakage Current	1.2IIN	uA	-100		+100	
Output High Voltage	1.2VOH	V	1.0		1.5	
Output Low Voltage	1.2VOL	V	-0.3		0.2	
Output High Current	1.2IOH	mA			-4	
Output Low Current	1.2IOL	mA	+4			
Input Capacitance	Ci	pF			10	
Optical transmitter Characteristics						
Signaling Rate for Each Lane （100GbE）		Gbps	-	25.78125		
Signaling Rate for Each Lane （OTU4）				27.95249		
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30		-	
Total Average Launch Power	Pt	dBm	-		+8.9	
Average Launch Power for Each Lane	Pa	dBm	-2.5		+2.9	2
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3		4.5	3
Transmitter and Dispersion Penalty for Each Lanes		TDP			1.5	
Average Launch Power of Off Transmitter for Each Lanes	Poff	dBm	-		-30	
Extinction Ratio	ER	dB	8			
$RIN_{20}OMA$		dB/Hz			-130	
Optical Return Loss Tolerance		dB			20	
Transmitter Reflectance		dB			-12	4
Eye Diagram		Compliant with IEEE 802.3ba-LR4/OTU4				
Optical receiver Characteristics						
Receive Rate for Each Lane(100GbE)		Gbps	-	25.78125		
Receive Rate for Each Lane(OTU4)				27.95249		
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Overload Input Optical Power	Pmax	dBm	5.5			5
Average Receive Power for Each Lane(100GE)	Pa	dBm	-20.9		4.5	6&7
Average Receive Power for Each Lane(OTU4)	Pa	dBm	-23.2		4.5	
Receive Power In OMA for Each Lane	PinOMA	dBm			4.5	
Difference in Receive Power between Any Two Lanes		dBm			4.5	
Receiver Sensitivity in OMA for Each Lane(100GbE) at BER= $1x10^{-12}$	S_{OMA}	dBm			-21.4	8

Equivalent receiver sensitivity (OTU4)	S_{AVG}	dBm		-23.2	9
Stressed Receiver Sensitivity in OMA for Each Lane(100GbE)		dBm		-17.9	10&11
Los Assert		dBm	-30		
Los De-assert		dBm		-20.9	
Los Hysteresis		dBm	0.5		

Note1. The supply current includes CFP module's supply current and test board working current.
Note2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
Note3. Even if the TDP<1dB, the OMA (min) must exceed this value
Note4. Transmitter reflectance is defined looking into the transmitter
Note5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
Note6. Minimum average receive power and maximum receiver sensitivity (OMA), each lane, is informative for 100GBase-LR4
Note7. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
Note8. Receiver sensitivity (OMA), each lane (max) is informative
Note9. Measured with PRBS 2^{31}-1 for BER=10^{-5}. The BER for the OTU4 application is required to be met only after FEC has been applied.
Note10. Measured with conformance test signal at TP3 for BER=10^{-12}
Note11. Conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB; stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Hardware Control Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
11	TX_DIS （PRG_CNTL）	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
14	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
16	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module
Note2: Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Hardware Alarm Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
12	RX_LOS （PRG_ALRM）	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100Ohm) is located within the CFP module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Management Interface Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
13	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
18	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
17	MDC	MDIO Clock	I	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
20	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register"Maximum High-Power-up ime"in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay	GLB_ALRMn_assert		150	ms	This is a logical

Time					"OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		20	ms	Value is dependent upon module start-up time.Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

High Speed Electrical Characteristics

Reference Clock Characteristics（optional）

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			161.1328125/644.53125		MHz	1/160 or 1/40 of electrical lane rate（100GE）
			174.7031 /698.8123MHz			1/160 or 1/40 of electrical lane rate（OTU4）
Frequency Stability	△f	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output	V_{DIFF}	400		1200	mV	Peak to Peak

Differential Voltage						Differential
RMS jitter[1,2]	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

CFP Register Allocation

CFP Register Allocation					
Staring Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 use
8000	807F	RO	128	8	CFP NVR 1.Basic ID register
8080	80FF	RO	128	8	CFP NVR 2.Extended ID register
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers
8180	81FF	RO	128	8	CFP NVR 4
8200	83FF	RO	4x128	N/A	MSA Reserved
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA
8800	887F	R/W	128	8	User NVR 1. User data registers
8880	88FF	R/W	128	8	User NVR 2. User data registers
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	RO	4096	N/A	Reserved for vendor private use
A000	A07F	R/W	128	16	CFP Module VR1. CFP Module level control and DDM registers
A080	A0FF	RO	128	16	Reserved by CFP MSA
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA
A200	A27F	R/W	128	16	etwork Lane VR 1.Network lane specific register
A280	A2FF	R/W	128	16	Network Lane VR 2.Network lane specific register
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA
A400	A47F	R/W	128	16	Host lane VR1. Host lane specific registers
A480	AFFF	RO	23x128	N/A	Reserved by CFP MSA

B000	FFFF	RO	5x4096	N/A	Reserved by CFP MSA

CFP NVR1

CFP NVR1

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8000	1	RO	7~0	Module Identifier	11	N/A
8001				Extended Identifier	A4	N/A
8002	1	RO	7~0	Connector Type Code	7	N/A
8003	1	RO	7~0	Ethernet Application Code	2	N/A
8004	1	RO	7~0	Fiber Channel Application Code	0	N/A
8005	1	RO	7~0	Copper Link Application Code	0	N/A
8006	1	RO	7~0	SONET/SDH Application Code	0	N/A
8007	1	RO	7~0	OTN Application Code	8	N/A
8008	1	RO	7~0	Additional Capable Rates Supported	18	N/A
8009	1	RO	7~0	Number of Lanes Supported	44	N/A
800A	1	RO	7~0	Media Properties	11	N/A
800B	1	RO	7~0	Maximum Network Lane Bit Rate	8C	0.2Gbps
800C	1	RO	7~0	Maximum host Lane Bit Rate	8C	0.2Gbps
800D	1	RO	7~0	Maximum Single Mode Optical Fiber Length	A	1km
800E	1	RO	7~0	Maximum Multi-Mode Mode Optical Fiber Length	0	10m
800F	1	RO	7~0	Maximum Copper Cable length	0	1m
8010	1	RO	7~0	Transmitter Spectral Characteristics1	1	N/A
8011	1	RO	7~0	Transmitter Spectral Characteristics2	4	N/A
8012	2	RO	7~0	Minimum Wavelength per Active Fiber	CA	25pm
8014	2	RO	7~0	Maximum Wavelength per Active Fibe	CC	25pm
8016	2	RO	7~0	Maximum per Lane Optical Width	0	1pm
8018	1	RO	7~0	Device Technology1	21	N/A
8019	1	RO	7~0	Device Technology2	44	N/A
801A	1	RO	7~0	Signal Code	40	N/A
801B	1	RO	7~0	Maximum Total Optical Output Power per Connector	70	100uW
801C	1	RO	7~0	Maximum Optical Input Power per Network Lane	1C	100uW
801D	1	RO	7~0	Maximum Power Consumption	2D	200mW
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode	64	20uW
801F	1	RO	7~0	Maximum Operating Case Temp Range	21	1degC
8020	1	RO	7~0	Minimum Operating Case Temp Range	0	1degC
8021	16	RO	7~0	Vendor Name	4F	N/A
8031	3	RO	7~0	Vendor OUI	0	N/A
8034	16	RO	7~0	Vendor Part Number	54	N/A
8044	16	RO	7~0	Vendor Serial Number	4A	N/A
8054	8	RO	7~0	Data Code	32	N/A
805C	2	RO	7~0	Lot Code	30	N/A
805E	10	RO	7~0	CLEI Code	30	N/A
8068	1	RO	7~0	CFP MSA hardware Specification Revision Number	0	N/A
8069	1	RO	7~0	CFP MSA Management Interface Specification Revision Number	16	
806A	2	RO	7~0	Module Hardware Version Number	1	N/A
806C	2	RO	7~0	Module Firmware Version Number	1	N/A

806E	1	RO	7~0	Digital Diagnostic Monitoring Type	C	N/A
806F	1	RO	7~0	Digital Diagnostic Monitoring Capability 1	3	N/A
8070	1	RO	7~0	Digital Diagnostic Monitoring Capability 2	F	N/A
8071	1	RO	7~0	Module Enhanced Options	68	N/A
8072	1	RO	7~0	Maximum High-Power-up Time	A	1sec
8073	1	RO	7~0	Maximum TX-Turn-on Time	1	1sec
8074	1	RO	7~0	Host Lane Signal Spec	C	N/A
8075	1	RO	7~0	Heat Sink Type	0	N/A
8076	1	RO	7~0	Maximum TX-Turn-off Time	1	1ms
8077	1	RO	7~0	Maximum High-Power-down Time	1	1sec
8078	1	RO	7~0	Module Enhanced Options 2	20	N/A
8079	1	RO	7~0	Transmitter Monitor Clock Options	7	N/A
807A	1	RO	7~0	Receiver Monitor Clock Options	7	0
807B	4	RO		Reserved	0	N/A
807F	1	RO	7~0	CFP NVR 1 Checksum	FD	N/A

CFP NVR2

Alarm/Warning Threshold Registers

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8080	2	RO	7~0	Transceiver Temp High Alarm Threshold	4B	1/256degC
8082	2	RO	7~0	Transceiver Temp High Warning Threshold	46	1/256degC
8084	2	RO	7~0	Transceiver Temp Low Warning Threshold	0	1/256degC
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold	0	1/256degC
8088	2	RO	7~0	VCC High Alarm Threshold	8C	0.1mV
808A	2	RO	7~0	VCC High Warning Threshold	88	0.1mV
808C	2	RO	7~0	VCC Low Warning Threshold	79	0.1mV
808E	2	RO	7~0	VCC Low Alarm Threshold	75	0.1mV
8090	2	RO	7~0	SOA Bias Current High Alarm Threshold	5091	8uA
8092	2	RO	7~0	SOA Bias Current High Warning Threshold	4E20	8uA
8094	2	RO	7~0	SOA Bias Current Low Warning Threshold	2710	8uA
8096	2	RO	7~0	SOA Bias Current Low Alarm Threshold	249F	8uA
8098	2	RO	7~0	Auxiliary 1 Monitor High Alarm Threshold	0	TBD
809A	2	RO	7~0	Auxiliary 1 Monitor High Warning Threshold	0	TBD
809C	2	RO	7~0	Auxiliary 1 Monitor Low Warning Threshold	0	TBD
809E	2	RO	7~0	Auxiliary 1 Monitor Low Alarm Threshold	0	TBD
80A0	2	RO	7~0	Auxiliary 2 Monitor High Alarm Threshold	0	TBD
80A2	2	RO	7~0	Auxiliary 2 Monitor High Warning Threshold	0	TBD
80A4	2	RO	7~0	Auxiliary 2 Monitor Low Warning Threshold	0	TBD
80A6	2	RO	7~0	Auxiliary 2 Monitor Low Alarm Threshold	0	TBD
80A8	2	RO	7~0	Laser Bias Current High Alarm Threshold	AF	SeeA2A0h
80AA	2	RO	7~0	Laser Bias Current High Warning Threshold	92	SeeA2A0h
80AC	2	RO	7~0	Laser Bias Current Low Warning Threshold	44	SeeA2A0h
80AE	2	RO	7~0	Laser Bias Current Low Alarm Threshold	30	SeeA2A0h
80B0	2	RO	7~0	Laser Output Power High Alarm Threshold	5F	SeeA2B0h or B330h
80B2	2	RO	7~0	Laser Output Power High Warning Threshold	55	SeeA2B0h or B330h
80B4	2	RO	7~0	Laser Output Power Low Warning Threshold	13	SeeA2B0h or B330h
80B6	2	RO	7~0	Laser Output Power Low Alarm Threshold	11	SeeA2B0h or B330h
80B8	2	RO	7~0	Laser Temperature High Alarm Threshold	41	SeeA2C0h

80BA	2	RO	7~0	Laser Temperature High Warning Threshold	3C	SeeA2C0h
80BC	2	RO	7~0	Laser Temperature Low Warning Threshold	28	SeeA2C0h
80BE	2	RO	7~0	Laser Temperature Low Alarm Threshold	23	SeeA2C0h
80C0	2	RO	7~0	Receive Optical Power High Alarm Threshold	AE7C	SeeA2D0h
80C2	2	RO	7~0	Receive Optical Power High Warning Threshold	6E18	SeeA2D0h
80C4	2	RO	7~0	Receive Optical Power Low Warning Threshold	51	SeeA2D0h
80C6	2	RO	7~0	Receive Optical Power Low Alarm Threshold	33	SeeA2D0h
80C8	55	RO	7~0	Reserved	0	TBD
80FF	1	RO	7~0	CFP NVR 2 Checksum	2E	N/A

CFP NVR3

Network Lane BOL Measurement Registers

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8100	32	RO	7~0	Rx Sensitivity Spec for network lanes 0~15	F9	0.01dBm
8120	32	RO	7~0	Tx Power Spec for network lanes 0~15	FF	0.01dBm
8140	32	RO	7~0	Measured ER for network lanes 0~15	3	0.01dB
8160	32	RO	7~0	Path Penalty for network lanes 0~15	0	0.01dB

CFP NVR4

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8180	1	RO	7~0	CFP NVR3 Checksum	E	N/A
8181	127	RO	7~1	Reserved	0	10m

CFP VR1

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Module Command/Setup Registers						
A000	2	RO	15~0	Reserved	0000h	
A002	2	RO	15~0	Reserved	0000h	
A004	1	RO		**NVR Access Control**	0000h	
			8~6	Reserved		
			4	Reserved		
			3~2	Command Status		
		RW	15~9	Reserved		
			5	User Restore and Save Command		
			1~0	Extended Commands		
A005	1	RO		**PRG_CNTL3 Function Select**	0000h	
			15~8	Reserved		
		RW	7~0	Function Select Code		
A006	1	RO		**PRG_CNTL2 Function Select**	0000h	
			15~8	Reserved		
		RW	7~0	Function Select Code		
A007	1	RO		**PRG_CNTL1 Function Select**	0001h	
			15~8	Reserved		
		RW	7~0	Function Select Code		
A008	1	RO		**PRG_ALRM3 Source Select**	0003h	
			15~8	Reserved		

		RW	7~0	Alarm Source Code		
A009	1	RO		**PRG_ALRM2 Source Select**	0002h	
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO		**PRG_ALRM1 Source Select**	0001h	
			15~8	Reserved	00h	
		RW	7~0	Alarm Source Code	00h	
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select	0000h	
			15~3	Reserved	0	
		RW	2~0	Module Bi/uni-Direction Mode Select	00b	
A00C	4	RO		Reserved	0000h	
Module Control Registers						
A010	1			**Module General Control**	0000h	
		RW/SC/LH	15	Soft Module Reset	0	
		RW	14	Soft Module Low Power	0	
		RW	13	Soft TX Disable	0	
		RW	12	Soft PRG_CNTL3 Control	0	
		RW	11	Soft PRG_CNTL2 Control	0	
		RW	10	Soft PRG_CNTL1 Control	0	
		RW	9	Soft GLB_ALRM Test	0	
		RO	8~6	Reserved	0	
		RO	5	TX_DIS Pin State	0	
		RO	4	MOD_LOPWR Pin State	0	
		RO	3	PRG_CNTL3 Pin State	0	
		RO	2	PRG_CNTL2 Pin State	0	
		RO	1	PRG_CNTL1 Pin State	0	
		RO	0	Reserved	0	
A011	1			**Netwowk Lane TX Control**	0200h	
		RO	15	Reserved	0	
		RW	14	TX PRBS Generator Enable	0	
		RW	13	TX PRBS Pattern 1	00b	
		RW	12	TX PRBS Pattern 0	00b	
		RW	11	TX De-skew Enable	0	
		RW	10	TX FIFO Reset	0	
		RW	9	TX FIFO Auto Reset	1	
		RW	8	TX Reset	0	
		RW	7~5	TX MCLK Control	000b	
		RO	4	Reserved	0	
		RW	3~1	TX Rate Select (10G lane rate)	000b or 110b	
		RW	0	TX Reference CLK Rate Select	1b	
A012	1			**Network Lane RXControl**	0200h	
		RW	15	Active Decision Voltageand Phase function	0b	
		RW	14	RX PRBS CheckerEnable	0b	
		RW	13	RX PRBS Pattern 1	00b	
		RW	12	RX PRBS Pattern 0	00b	
		RW	11	RX Lock RX_MCLK to Reference CLK	0b	
		RW	10	Network Lane Loop-back	0b	
		RW	9	RX FIFO Auto Reset	1b	
		RW	8	RX Reset	0b	
		RW	7~5	RX MCLK Control	000b	
		RW	4	RX FIFO Reset	0b	
		RW	3~1	RX Rate Select	000b	
		RW	0	RX Reference CLK Rate Select	1b	

A013	1	RW		**Individual Network Lane TX_DIS Control**	0000h	
			15	Lane 15 Disable	0	
			14	Lane 14 Disable	0	
			13	Lane 13 Disable	0	
			12	Lane 12 Disable	0	
			11	Lane 11 Disable	0	
			10	Lane 10 Disable	0	
			9	Lane 9 Disable	0	
			8	Lane 8 Disable	0	
			7	Lane 7 Disable	0	
			6	Lane 6 Disable	0	
			5	Lane 5 Disable	0	
			4	Lane 4 Disable	0	
			3	Lane 3 Disable	0	
			2	Lane 2 Disable	0	
			1	Lane 1 Disable	0	
			0	Lane 0 Disable	0	
A014	1			**Host Lane Control**	0000h	
		RO	15	Reserved	0	
		RW	14	TX PRBS Checker Enable	0	
		RW	13	TX PRBS Pattern 1	000b	
		RW	12	TX PRBS Pattern 0	000b	
		RO	11	Reserved	000b	
		RW	10	Host Lane Loop-back Enable	0	
		RO	9	Reserved	0	
		RO	8	Reserved	0	
		RW	7	RX PRBS Generator Enable	0	
		RW	6	RX PRBS Pattern 2	000b	
		RW	5	RX PRBS Pattern 1	000b	
		RW	4	RX PRBS Pattern 0	000b	
		RO	3~0	Reserved	0h	
A015	1	RO		Reserved	0000h	
A016	1	RO		**Module State**	0000h	
			15~9	Reserved	0	
			8	High-Power-down State	0	
			7	TX-Turn-off State	0	
			6	Fault State	0	
			5	Ready State	0	
			4	TX-Turn-on State	0	
			3	TX-Off State	0	
			2	High-Power-up State	0	
			1	Low-Power State	0	
			0	Initialize State	0	
A017	1	RO		Reserved	0000h	
A018	1	RO		**Global Alarm Summary**	0000h	
			15	GLB_ALRM Assertion Status	0	
			14	Host Lane Fault and Status Summary	0	
			13	Network Lane Fault and Status Summary	0	
			12	Network Lane Alarm and Warning Summary	0	
			11	Module Alarm and Warning 2 Summary	0	
			10	Module Alarm and Warning 1	0	

				Summary		
			9	Module Fault Summary	0	
			8	Module General Status Summary	0	
			7	Module State Summary	0	
			6~1	Reserved	0	
			0	Soft GLB_ALRM Test Status	0	
A019	1	RO		**Network Lane Alarm and Warning Summary**	0000h	
			15	Lane 15 Alarm and Warning Summary	0	
			14	Lane 14 Alarm and Warning Summary	0	
			13	Lane 13 Alarm and Warning Summary	0	
			12	Lane 12 Alarm and Warning Summary	0	
			11	Lane 11 Alarm and Warning Summary	0	
			10	Lane 10 Alarm and Warning Summary	0	
			9	Lane 9 Alarm and Warning Summary	0	
			8	Lane 8 Alarm and Warning Summary	0	
			7	Lane 7 Alarm and Warning Summary	0	
			6	Lane 6 Alarm and Warning Summary	0	
			5	Lane 5 Alarm and Warning Summary	0	
			4	Lane 4 Alarm and Warning Summary	0	
			3	Lane 3 Alarm and Warning Summary	0	
			2	Lane 2 Alarm and Warning Summary	0	
			1	Lane 1 Alarm and Warning Summary	0	
			0	Lane 0 Alarm and Warning Summary	0	
A01A	1	RO		**Network Lane Fault and Status Summary**	0000h	
			15	Lane 15 Fault and Status Summary	0	
			14	Lane 14 Fault and Status Summary	0	
			13	Lane 13 Fault and Status Summary	0	
			12	Lane 12 Fault and Status Summary	0	
			11	Lane 11 Fault and Status Summary	0	
			10	Lane 10 Fault and Status Summary	0	
			9	Lane 9 Fault and Status Summary	0	
			8	Lane 8 Fault and Status Summary	0	
			7	Lane 7 Fault and Status Summary	0	
			6	Lane 6 Fault and Status Summary	0	
			5	Lane 5 Fault and Status Summary	0	
			4	Lane 4 Fault and Status Summary	0	
			3	Lane 3 Fault and Status Summary	0	
			2	Lane 2 Fault and Status Summary	0	
			1	Lane 1 Fault and Status Summary	0	
			0	Lane 0 Fault and Status Summary	0	
A01B	1	RO		**Host Lane Fault and Status Summary**	0000h	
			15	Lane 15 Fault and Status Summary	0	
			14	Lane 14 Fault and Status Summary	0	
			13	Lane 13 Fault and Status Summary	0	
			12	Lane 12 Fault and Status Summary	0	
			11	Lane 11 Fault and Status Summary	0	
			10	Lane 10 Fault and Status Summary	0	
			9	Lane 9 Fault and Status Summary	0	

			8	Lane 8 Fault and Status Summary	0	
			7	Lane 7 Fault and Status Summary	0	
			6	Lane 6 Fault and Status Summary	0	
			5	Lane 5 Fault and Status Summary	0	
			4	Lane 4 Fault and Status Summary	0	
			3	Lane 3 Fault and Status Summary	0	
			2	Lane 2 Fault and Status Summary	0	
			1	Lane 1 Fault and Status Summary	0	
			0	Lane 0 Fault and Status Summary	0	
A01C	1	RO		Reserved	0	
Module FAWS Registers						
A01D	1	RO		**Module General Status**	0000h	
			15	Reserved	0	
			14	Reserved	0	
			13	HW_Interlock	0	
			12~11	Reserved	0	
			10	Loss of REFCLK Input	0	
			9	TX_JITTER_PLL_LOL	0	
			8	TX_CMU_LOL	0	
			7	TX_LOSF	0	
			6	TX_HOST_LOL	0	
			5	RX_LOS	0	
			4	RX_NETWORK_LOL	0	
			3	Out of Alignment	0	
			2	Reserved	0	
			1	HIPWR_ON	0	
			0	Reserved	0	
A01E	1	RO		**Module Fault Status**	0000h	
			15	Reserved	0	
			14~7	Reserved	0	
			6	PLD or Flash Initialization Fault	0	
			5	Power Supply Fault	0	
			4~2	Reserved	000b	
			1	CFP Checksum Fault	0	
			0	Reserved	0	
A01F	1	RO		**Module Alarms and Warnings 1**	0000h	
			15~12	Reserved	000b	
			11	Mod Temp High Alarm	0	
			10	Mod Temp High Warning	0	
			9	Mod Temp Low Warning	0	
			8	Mod Temp Low Alarm	0	
			7	Mod Vcc High Alarm	0	
			6	Mod Vcc High Warning	0	
			5	Mod Vcc Low Warning	0	
			4	Mod Vcc Low Alarm	0	
			3	Mod SOA Bias High Alarm	0	
			2	Mod SOA Bias High Warning	0	
			1	Mod SOA Bias Low Warning	0	
			0	Mod SOA Bias Low Alarm	0	
A020	1	RO		**Module Alarms and Warnings 2**	0000h	
			15~8	Reserved	0	
			7	Mod Aux 1 High Alarm	0	
			6	Mod Aux 1 High Warning	0	
			5	Mod Aux 1 Low Warning	0	
			4	Mod Aux 1 Low Alarm	0	
			3	Mod Aux 2 High Alarm	0	

			2	Mod Aux 2 High Warning	0	
			1	Mod Aux 2 Low Warning	0	
			0	Mod Aux 2 Low Alarm	0	
A021	1	RO		Reserved	0000h	
A022	1			**Module State Latch**	0000h	
		RO	15~9	Reserved	0	
		RO/LH/COR	8	High-Power-down State Latch	0	
		RO/LH/COR	7	TX-Turn-off State Latch	0	
		RO/LH/COR	6	Fault State Latch	0	
		RO/LH/COR	5	Ready State Latch	0	
		RO/LH/COR	4	TX-Turn-on State Latch	0	
		RO/LH/COR	3	TX-Off State Latch	0	
		RO/LH/COR	2	High-Power-up State Latch	0	
		RO/LH/COR	1	Low-Power State Latch	0	
		RO/LH/COR	0	Initialize State Latch	0	
A023	1			**Module General Status Latch**	0000h	
		RO	15	Reserved	0	
		RO	14	Reserved	0	
		RO/LH/COR	13	HW_Interlock Latch	0	
		RO	12~11	Reserved	0	
		RO/LH/COR	10	Loss of REFCLK Input Latch	0	
		RO/LH/COR	9	TX_JITTER_PLL_LOL Latch	0	
		RO/LH/COR	8	TX_CMU_LOL Latch	0	
		RO/LH/COR	7	TX_LOSF Latch	0	
		RO/LH/COR	6	TX_HOST_LOL Latch	0	
		RO/LH/COR	5	RX_LOS Latch	0	
		RO/LH/COR	4	RX_NETWORK_LOL Latch	0	
		RO/LH/COR	3	Out of Alignment Latch	0	
		RO	2~0	Reserved	000b	
A024	1			**Module Fault Status latch**	0000h	
		RO	15~7	Reserved	0	
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch	0	
		RO/LH/COR	5	Power Supply Fault Latch	0	
		RO	4~2	Reserved	000b	
		RO/LH/COR	1	CFP Checksum Fault Latch	0	
		RO	0	Reserved	0	
A025	1			**Module Alarms and Warnings 1 Latch**	0000h	
		RO	15~12	Reserved	0000b	
		RO/LH/COR	11	Mod Temp High Alarm Latch	0	
		RO/LH/COR	10	Mod Temp High Warning Latch	0	
		RO/LH/COR	9	Mod Temp Low Warning Latch	0	
		RO/LH/COR	8	Mod Temp Low Alarm Latch	0	
		RO/LH/COR	7	Mod Vcc High Alarm Latch	0	
		RO/LH/COR	6	Mod Vcc High Warning Latch	0	
		RO/LH/COR	5	Mod Vcc Low Warning Latch	0	
		RO/LH/COR	4	Mod Vcc Low Alarm Latch	0	
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch	0	
		RO/LH/COR	2	Mod SOA Bias High Warning Latch	0	
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch	0	
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch	0	
A026	1			**Module Alarms and Warnings 2 latch**	0	
		RO	15~8	Reserved	0	
		RO/LH/COR	7	Mod Aux 1 High Alarm Latch	0	
		RO/LH/COR	6	Mod Aux 1 High Warning Latch	0	

		RO/LH/COR	5	Mod Aux 1 Low Warning Latch	0	
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch	0	
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch	0	
		RO/LH/COR	2	Mod Aux 2 High Warning Latch	0	
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch	0	
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch	0	
A027	1	RO		Reserved	0000h	
A028	1			**Module Stable Enable**	006Ah	
		RO	15~9	Reserved	0	
		RW	8	High-Power-down State Enable	0	
		RW	7	TX-Turn-off State Enable	0	
		RW	6	Fault State Enable	1	
		RW	5	Ready State Enable	1	
		RW	4	TX-Turn-on State Enable	0	
		RW	3	TX-Off State Enable	1	
		RW	2	High-Power-up State Enable	0	
		RW	1	Low-Power State Enable	1	
		RO	0	Initialize State Enable	0	
A029	1			**Module General Status Enable**	A7F8h	
		RW	15	GLB_ALRM Master Enable	1	
		RO	14	Reserved	0	
		RW	13	HW Interlock	1	
		RO	12~11	Reserved	0	
		RW	10	Loss of REFCLK Input Enable	1	
		RW	9	TX_JITTER_PLL_LOL Enable	1	
		RW	8	TX_CMU_LOL Enable	1	
		RW	7	TX_LOSF Enable	1	
		RW	6	TX_HOST_LOL Enable	1	
		RW	5	RX_LOS Enable	1	
		RW	4	RX_NETWORK_LOL Enable	1	
		RW	3	Out of Alignment Enable	1	
		RO	2~0	Reserved	000b	
A02A	1			**Module Fault Status Enable**	0062h	
		RO	15~7	Reserved	0	
		RW	6	PLD or Flash Initialization Fault Enable	1	
		RW	5	Power Supply Fault Enable	1	
		RO	4~2	Reserved	000b	
		RW	1	CFP Checksum Fault Enable	1	
		RO	0	Reserved	0	
A02B	1	RO		Module Alarm and Warnings 1 Enable	0FFFh	
			15~12	Reserved	0000b	
			11	Mod Temp Hi Alarm Enable	1	
			10	Mod Temp Hi Warn Enable	1	
			9	Mod Temp Low Warning Enable	1	
			8	Mod Temp Low Alarm Enable	1	
			7	Mod Vcc High Alarm Enable	1	
			6	Mod Vcc High Warning Enable	1	
			5	Mod Vcc Low Warning Enable	1	
			4	Mod Vcc Low Alarm Enable	1	
			3	Mod SOA Bias High Alarm Enable	1	
			2	Mod SOA Bias High Warning Enable	1	
			1	Mod SOA Bias Low Warning Enable	1	
			0	Mod SOA Bias Low Alarm Enable	1	

A02C	1			**Module Alarms and Warnings Enable**	**00FFh**	
		RO	15~8	Reserved	00h	
		RW	7	Mod Aux 1 High Alarm Enable	1	
			6	Mod Aux 1 High Warning Enable	1	
			5	Mod Aux 1 Low Warning Enable	1	
			4	Mod Aux 1 Low Alarm Enable	1	
			3	Mod Aux 2 High Alarm Enable	1	
			2	Mod Aux 2 High Warning Enable	1	
			1	Mod Aux 2 Low Warning Enable	1	
			0	Mod Aux 2 Low Alarm Enable	1	
A02D	2	RO		Reserved	0000h	
Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value	0000h	
A030	1	RO	15~0	Module Power supply	0000h	
				3.3 V Monitor A/D Value	0000h	
A031	1	RO	15~0	SOA Bias Current A/D Value	0000h	
A032	1	RO	15~0	Module Auxiliary 1 Monitor A/D Value	0000h	
A033	1	RO	15~0	Module Auxiliary 2 Monitor A/D Value	0000h	
A034	4	RO		Reserved		
Module PRBS Registers						
A038	1	RO		**Network Lane PRBS Data Bit Count**	0000h	
			15~10	Exponent	0	
			9~0	Mantissa	0	
A039	1	RO		**Host Lane PRBS Data Bit Count**	0000h	
			15~10	Exponent	0	
			9~0	Mantissa	0	
A03A	70	RO		Reserved	0	

CFP Network Lane VR1

Network Lane VR1

Network Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Network Lane FAWS Registers						
A200	16	RO		**Network Lane n Alarm and Warning**	0000h	
			15	Bias High Alarm	0	
			14	Bias High Warning	0	
			13	Bias Low Warning	0	
			12	Bias Low Alarm	0	
			11	TX Power High Alarm	0	
			10	TX Power High Warning	0	
			9	TX Power Low Warning	0	
			8	TX Power Low Alarm	0	
			7	Laser Temperature High Alarm	0	
			6	Laser Temperature High Warning	0	
			5	Laser Temperature Low Warning	0	
			4	Laser Temperature Low Alarm	0	
			3	RX Power High Alarm	0	
			2	RX Power High Warning	0	
			1	RX Power Low Warning	0	
			0	RX Power Low Alarm	0	

A210	16	RO		**Network Lane n Fault and Status**	0000h	
			15	Lane TEC Fault	0	
			14	Lane Wavelength Unlocked Fault	0	
			13	Lane APD Power Supply Fault	0	
			12~8	Reserved	0	
			7	Lane TX_LOSF	0	
			6	Lane TX_LOL	0	
			5	Reserved	0	
			4	Lane RX_LOS	0	
			3	Lane RX_LOL	0	
			2	Lane RX FIFO error	0	
			1	Reserved	0	
			0	Reserved	0	
Network Lane FAWS Latch Registers						
A220	16	RO/LH/COR		**Network Lane n Alarm and Warning Latch**	0000h	
			15	Bias High Alarm Latch	0000h	
			14	Bias High Warning Latch	0	
			13	Bias Low Warning Latch	0	
			12	Bias Low Alarm Latch	0	
			11	TX Power High Alarm Latch	0	
			10	TX Power High Warning Latch	0	
			9	TX Power Low Warning Latch	0	
			8	TX Power Low Alarm Latch	0	
			7	Laser Temperature High Alarm Latch	0	
			6	Laser Temperature High Warning Latch	0	
			5	Laser Temperature Low Warning Latch	0	
			4	Laser Temperature Low Alarm Latch	0	
			3	RX Power High Alarm Latch	0	
			2	RX Power High Warning Latch	0	
			1	RX Power Low Warning Latch	0	
			0	RX Power Low Alarm Latch	0	
A230	16	RO/LH/COR		Network Lane n Fault and Status latch	0000h	
			15	Lane TEC Fault Latch	0	
			14	Lane Wavelength Unlocked Fault Latch	0	
			13	Lane APD Power Supply Fault Latch	0	
			12~8	Reserved	0	
			7	Lane TX_LOSF Latch	0	
			6	Lane TX_LOL Latch	0	
			5	Reserved	0	
			4	Lane RX_LOS Latch	0	
			3	Lane RX_LOL Latch	0	
			2	Lane RX FIFO Status Latch	0	
		RO	1~0	Reserved	0	
A240	16	RW		**Network Lane n Alarm and Warning Enable**	FFFFh	
			15	Bias High Alarm Enable	1	
			14	Bias High Warning Enable	1	
			13	Bias Low Warning Enable	1	
			12	Bias Low Alarm Enable	1	
			11	TX Power High Alarm Enable	1	
			10	TX Power High Warning Enable	1	

			9	TX Power Low Warning Enable	1	
			8	TX Power Low Alarm Enable	1	
			7	Laser Temperature High Alarm Enable	1	
			6	Laser Temperature High Warning Enable	1	
			5	Laser Temperature Low Warning Enable	1	
			4	Laser Temperature Low Alarm Enable	1	
			3	RX Power High Alarm Enable	1	
			2	RX Power High Warning Enable	1	
			1	RX Power Low Warning Enable	1	
			0	RX Power Low Alarm Enable	1	
A250	16			**Network Lane n Fault and Status Enable**	E0DCh	
		RW	15	Lane TEC Fault Enable	1	
		RW	14	Lane Wavelength Unlocked Fault Enable	1	
		RW	13	Lane APD Power Supply Fault Enable	1	
		RO	12~8	Reserved	0	
		RW	7	Lane TX_LOSF Enable	1	
		RW	6	Lane TX_LOL Enable	1	
		RO	5	Reserved	0	
		RW	4	Lane RX_LOS Enable	1	
		RW	3	Lane RX_LOL Enable	1	
		RW	2	Lane RX FIFO Status Enable	1	
		RO	1~0	Reserved	0	
A260	32	RO		Reserved	0000h	

CFP Network Lane VR2

Network Lane VR2

Network Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Network Lane Control Registers						
A280	16			**Network Lane n FEC Controls**	0000h	
		RW	15~8	Phase Adjustment	00h	
		RW	7~0	Amplitude Adjustment	00h	
A290	16	RO	15~0	Network Lane n PRBS Rx Error Count	0000h	
			15~10	Exponent	0	
			9~0	Mantissa	0	
Network Lane A/D value Measurement Registers						
A2A0	16	RO	15~0	Network Lane n Laser Bias Current monitor A/D value	0000h	
A2B0	16	RO	15~0	Network Lane n Laser Output Power monitor A/D value	0000h	
A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value	0000h	
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value	0000h	
A2E0	32	RO	15~0	Reserved	0000h	

CFP Host lane Lane VR1

Host Lane VR1

Host Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Host Lane FAWS Status Registers						
A400	16			**Host Lane m Fault and Status**	0000h	
		RO	15~2	Reserved	0	
		RO	1	Lane TX FIFO Error	0	
		RO	0	TX_HOST_LOL	0	
Host Lane FAWS Latch Registers						
A410	16			**Host Lane m Fault and Status Latch**	0000h	
		RO	15~2	Reserved	0	
		RO/LH/COR	1	Lane TX FIFO Error Latch	0	
		RO/LH/COR	0	TX_HOST_LOL Latch	0	
Host Lane FAWS Enable Registers						
A420	16			**Host Lane m Fault and Status Enable**	0001h	
		RO	15~2	Reserved	0	
		RW	1	Lane TX FIFO Error Enable	0	
		RW	0	TX_HOST_LOL_Enable	1	
Host Lane Digital PRBS Register						
A430	16			**Host Lane m PRBS TX Error Count**	0000h	
		RO	15~10	Exponent	0	
		RW	9~0	Mantissa	0	
Host Lane Control Registers						
A440	16			**Host Lane m Control**	0007h	
		RO	15~4	Reserved	0000b	
		RW	3~0	Signal Pre/De-emphasis	0000b Or 0111b	
A450	48	RO		Reserved	0000	

Pin Description

The CFP2 connector has 104 pins which are arranged in Top and Bottom rows. The pin map is shown in table below. The detailed description of the Bottom row ranges from pin 1 through pin 52 and is shown Table below. The pin orientation is shown below in Figure below.

Figure : CFP2 Pin Map Orientation

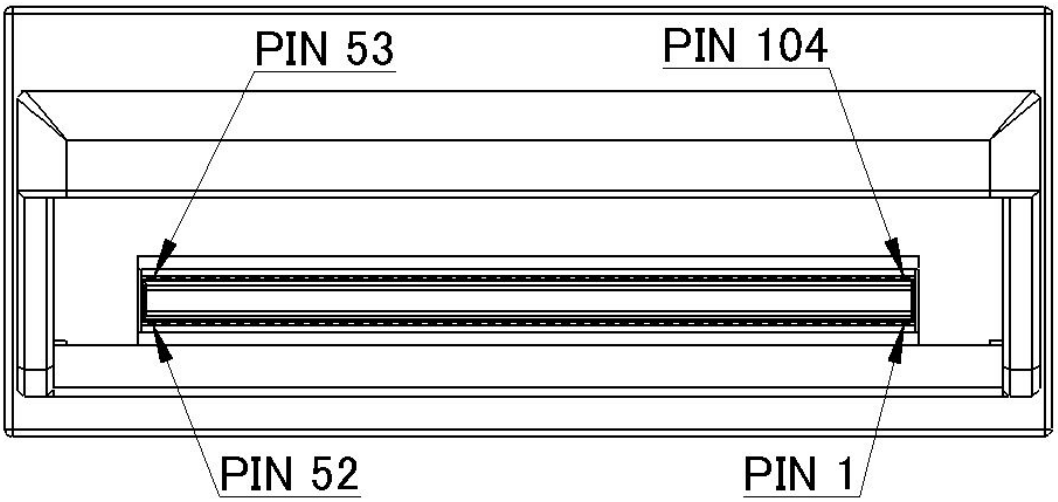


Table : CFP2 Pin-Map

1	GND	104	GND
2	*(TX_MCLKn)*	103	N.C.
3	*(TX_MCLKp)*	102	N.C.
4	GND	101	GND
5	N.C.	100	TX3n
6	N.C.	99	TX3p
7	3.3V_GND	98	GND
8	3.3V_GND	97	TX2n
9	3.3V	96	TX2p
10	3.3V	95	GND
11	3.3V	94	N.C.
12	3.3V	93	N.C.
13	3.3V_GND	92	GND
14	3.3V_GND	91	N.C.
15	VND_IO_A	90	N.C.
16	VND_IO_B	89	GND
17	PRG_CNTL1	88	TX1n
18	PRG_CNTL2	87	TX1p
19	PRG_CNTL3	86	GND
20	PRG_ALRM1	85	TX0n
21	PRG_ALRM2	84	TX0p
22	PRG_ALRM3	83	GND
23	GND	82	N.C.

24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V_GND
40	3.3V_GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V_GND
46	3.3V_GND
47	N.C.
48	N.C.
49	GND
50	*(RX_MCLKn)*
51	*(RX_MCLKp)*
52	GND

81	N.C.
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

Table: Pin description

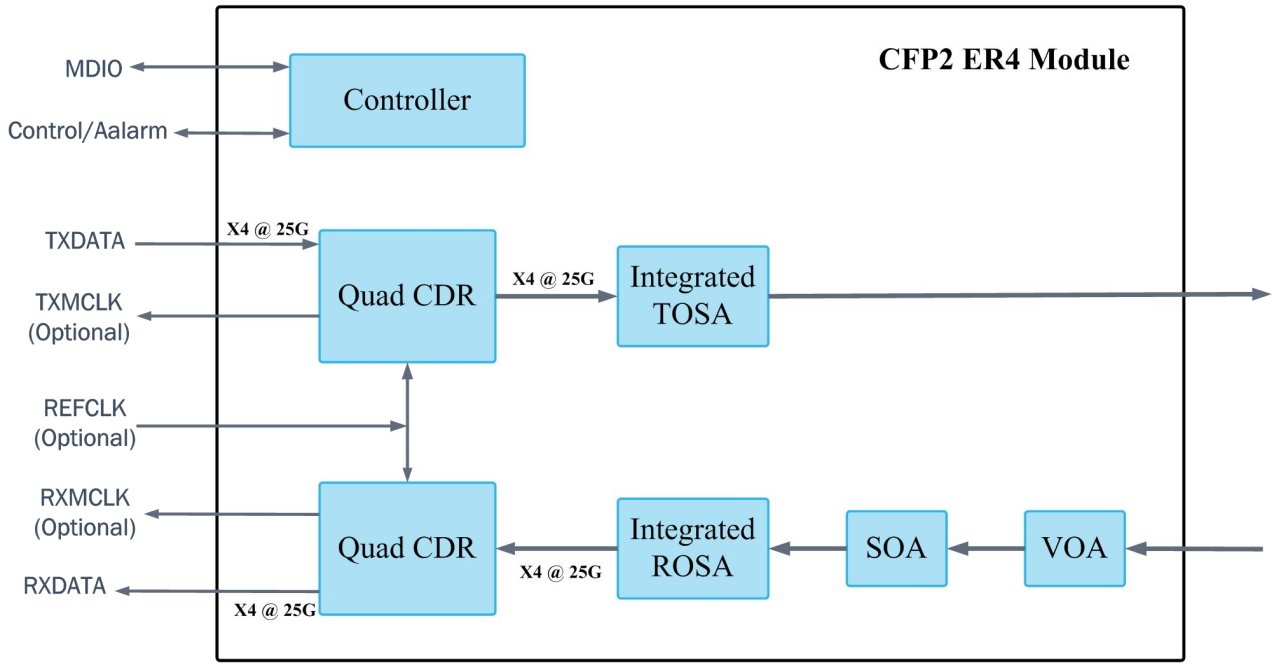
PIN#	Name	I/O	Logic	Description
1	GND			
2	*(TX_MCLKn)*	O	CML	For optical waveform testing. Not for normal use.
3	*(TX_MCLKp)*	O	CML	For optical waveform testing. Not for normal use.
4	GND			

5	**N.C.**			No Connect
6	**N.C.**			No Connect
7	**3.3V_GND**			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
8	**3.3V_GND**			
9	**3.3V**			3.3V Module Supply Votage
10	**3.3V**			
11	**3.3V**			
12	**3.3V**			
13	**3.3V_GND**			
14	**3.3V_GND**			
15	**VND_IO_A**	I/O		Module Vendor I/O A. Do Not Connect!
16	**VND_IO_B**	I/O		Module Vendor I/O B. Do Not Connect!
17	**PRG_CNTL1**	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
18	**PRG_CNTL2**	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO
19	**PRG_CNTL3**	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO
20	**PRG_ALRM1**	O	LVCMOS	Programmable Alarm 1 set over MDIO
21	**PRG_ALRM2**	O	LVCMOS	Programmable Alarm 2 set over MDIO
22	**PRG_ALRM3**	O	LVCMOS	Programmable Alarm 3 set over MDIO
23	**GND**			
24	**TX_DIS**	I	LVCMOS w/PUR	Transmitter Disable for all lanes, “1” or NC=transmitter disabled,”0”=transmitter enabled
25	**RX_LOS**	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	**MOD_LOPWR**	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	**MOD_ABS**	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	**MOD_RSTn**	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	**GLB_ALRMn**	O	LVCMOS	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	**GND**			
31	**MDC**	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	**MDIO**	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	**PRTADR0**	I	1.2V CMOS	MDIO Physical Port address bit 0

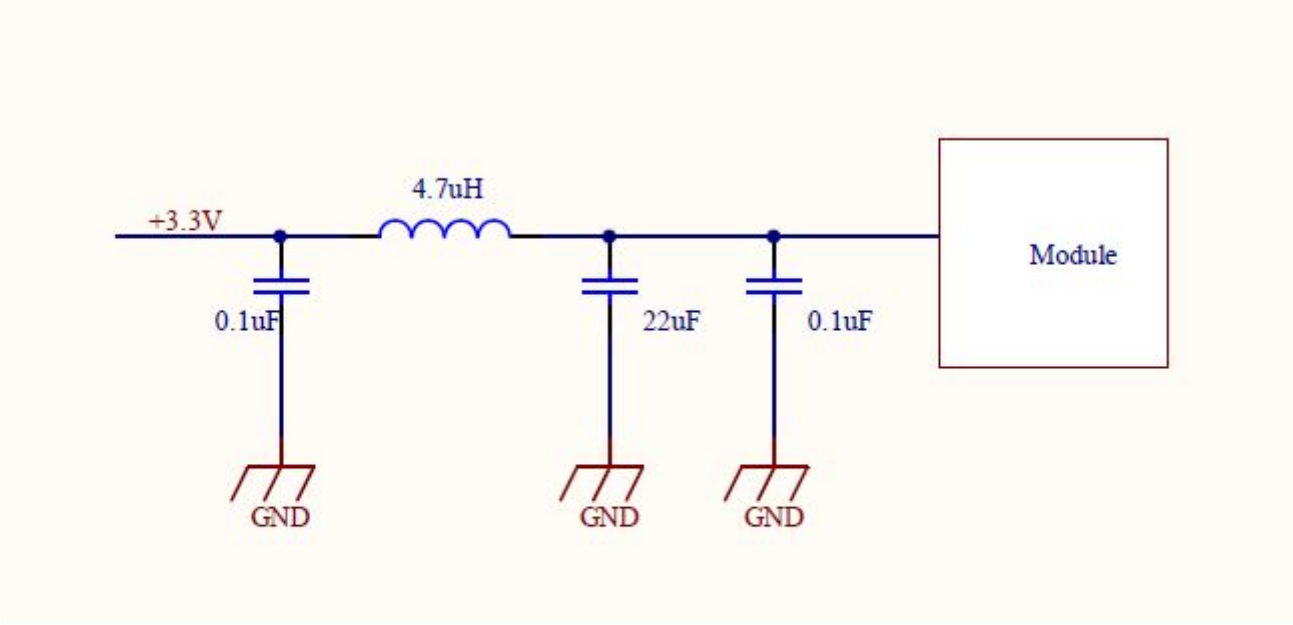
34	**PRTADR1**	I	1.2V CMOS	MDIO Physical Port address bit 1
35	**PRTADR2**	I	1.2V CMOS	MDIO Physical Port address bit 2
36	**VND_IO_C**	I/O		Module Vendor I/O C. Do Not Connect!
37	**VND_IO_D**	I/O		Module Vendor I/O D. Do Not Connect!
38	**VND_IO_E**	I/O		Module Vendor I/O E. Do Not Connect!
39	**3.3V_GND**			
40	**3.3V_GND**			
41	**3.3V**			3.3V Module Supply Voltage
42	**3.3V**			
43	**3.3V**			
44	**3.3V**			
45	**3.3V_GND**			
46	**3.3V_GND**			
47	**N.C.**			No Connect
48	**N.C.**			
49	**GND**			
50	***(RX_MCLKn)***	O	CML	For optical waveform testing. Not for normal use.
51	***(RX_MCLKp)***	O	CML	For optical waveform testing. Not for normal use.
52	**GND**			
53	**GND**			
54	**N.C.**			
55	**N.C.**			
56	**GND**			
57	**RX0p**	O	CML	Output Data
58	**RX0n**	O	CML	Inverted Output Data
59	**GND**			
60	**RX1p**	O	CML	Output Data
61	**RX1n**	O	CML	Inverted Output Data
62	**GND**			
63	**N.C.**			
64	**N.C.**			
65	**GND**			
66	**N.C.**			
67	**N.C.**			
68	**GND**			
69	**RX2p**	O	CML	Output Data

70	RX2n	O	CML	Inverted Output Data
71	GND			
72	RX3p	O	CML	Output Data
73	RX3n	O	CML	Inverted Output Data
74	GND			
75	N.C.			
76	N.C.			
77	GND			
78	(REFCLKp)			
79	(REFCLKn)			
80	GND			
81	N.C.			
82	N.C.			
83	GND			
84	TX0p	I	CML	Input Data
85	TX0n	I	CML	Inverted Input Data
86	GND			
87	TX1p	I	CML	Input Data
88	TX1n	I	CML	Inverted Input Data
89	GND			
90	N.C.			
91	N.C.			
92	GND			
93	N.C.			
94	N.C.			
95	GND			
96	TX2p	I	CML	Input Data
97	TX2n	I	CML	Inverted Input Data
98	GND			
99	TX3p	I	CML	Input Data
100	TX3n	I	CML	Inverted Input Data
101	GND			
102	N.C.			
103	N.C.			
104	GND			

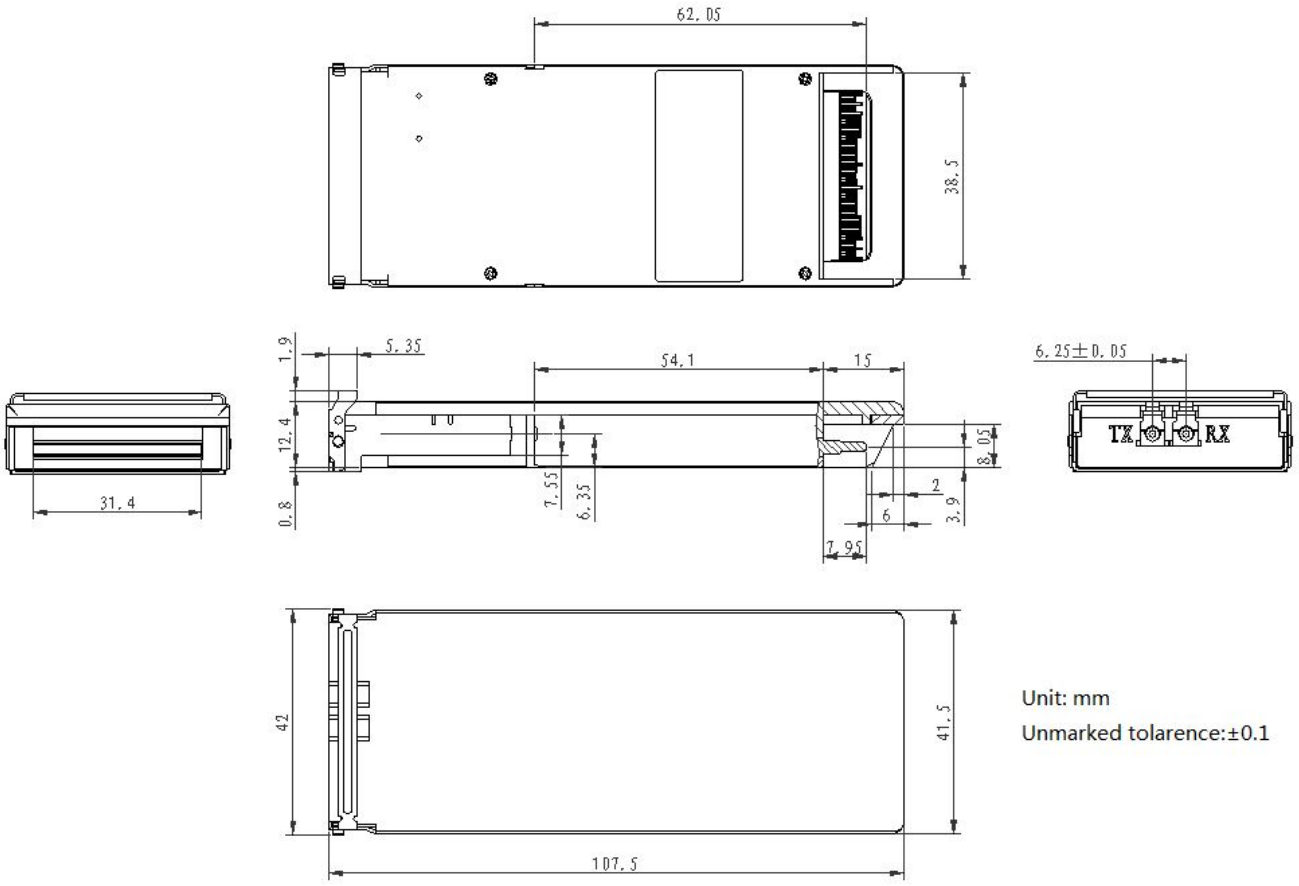
Block diagram



Required Host Board Components



Package outline



Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2 Class B	15kV air discharges during operation and 8kV direct contact discharge
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B CENELEC EN55022 VCCI Class 1	Compliant with standard

Immunity	IEC61000-4-3 Class 2	Compliant with any electo-magnetic regulations
Safety	FDA CDRH 21-CFR 1040 Class 1	
	UL	
	TUV-GS	
	CE	

Ordering Information

Part No	Specifications									Application Code
	Pack	Data rate	Tx	Pout	Rx	S	Top	Reach	Others	
RTXM290-608	CFP2	103.125Gbps ~112 Gbps	1310nm LAN Cooled EA DFB-LD	-2.5~+2.9 dBm	PIN	<-21.4dBm	0~70°C	40km	DDM	100GbE/OTU4