

QSFP+ Dual LC 40G SMF 2km Transceiver

AQOLBCQ4EDMA0776



Applications

- 40 Gigabit Ethernet (41.25Gbps)

Features

- QSFP+ Type Dual LC Transceiver
- 4 x CWDM – 1271/1291/1311/1331 nm
- PIN Photo Detector
- -5°C to +70°C case operating temperature range
- 2Km transmission with SMF
- 3.3V power supply
- Power consumption < 3.5W
- Compliant with QSFP+ MSA SFF-8436
- Hot pluggable
- Serial ID information support
- Digital diagnostic functions (Via I²C)
- Compliant with RoHS
- Compliant with UL & TUV

Ordering Information

Form Factor	Date Rate	MZDia	Distance	Wavelength (nm)	TX Power (each lane) (dBm)	RX Sensitivity (each lane) (dBm)	Voltage (V)	Coupling	DDM (Y/N)	Temperature (°C)	Part Number
QSFP+ Dual LC	40G	SMF	2km	1271 nm 1291 nm 1311 nm 1331 nm	-7 ~ 2.3	<-11.5	3.3	AC/AC	Y	-5 ~ +70	AQOLBCQ4EDMA0776

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Storage Temperature	T_S	--	-40	+85	°C
Storage Relative Humidity	RH	Non condensing	0	85	%
Supply Voltage # 3.3	V_{CC}	--	0	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature (Case)	T_C	--	-5	--	70	°C
Supply Voltage	V_{CC}	--	3.13	3.3	3.47	V
Supply Current	I_{CC}	--	--	--	1000	mA
Data Rate	DR	--	--	41.25	--	Gbps
Distance		--	0.02	--	2	km

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transmitter						
Differential Input Impedance	R_{DI}	--	--	100	--	Ohm
High speed Differential Input Voltage (CML)	V_{CML_DI}	AC-Coupled, peak to peak	0.2	--	1.0	V
Low speed Input Voltage - Low (LVCOMS)	V_{LVCMOS_IL}	--	-0.3	--	$V_{CC} * 0.3$	V
Low speed Input Voltage - High (LVCOMS)	V_{LVCMOS_IH}	--	$V_{CC} * 0.7$	--	$V_{CC} + 0.5$	V
Low speed Input Voltage - Low (LVTTTL)	V_{LVTTTL_IL}	--	-0.3	--	0.8	V
Low speed Input Voltage - High (LVTTTL)	V_{LVTTTL_IH}	--	2	--	$V_{CC} + 0.3$	V
Receiver						
Differential Output Impedance	R_{DO}	--	--	100	--	Ohm
High speed Differential Output Voltage (CML)	V_{CML_DO}	AC-Coupled, peak to peak	0.3	--	0.8	V
Low speed Output Voltage - Low (LVCOMS)	V_{LVCMOS_OL}	--	0	--	0.4	V
Low speed Output Voltage - High (LVCOMS)	V_{LVCMOS_OH}	--	$V_{CC} - 0.5$	--	$V_{CC} + 0.3$	V
Low speed Output Voltage - Low (LVTTTL)	V_{LVTTTL_OL}	--	0	--	0.4	V
Low speed Output Voltage - High (LVTTTL)	V_{LVTTTL_OH}	--	$V_{CC} - 0.5$	--	$V_{CC} + 0.3$	V

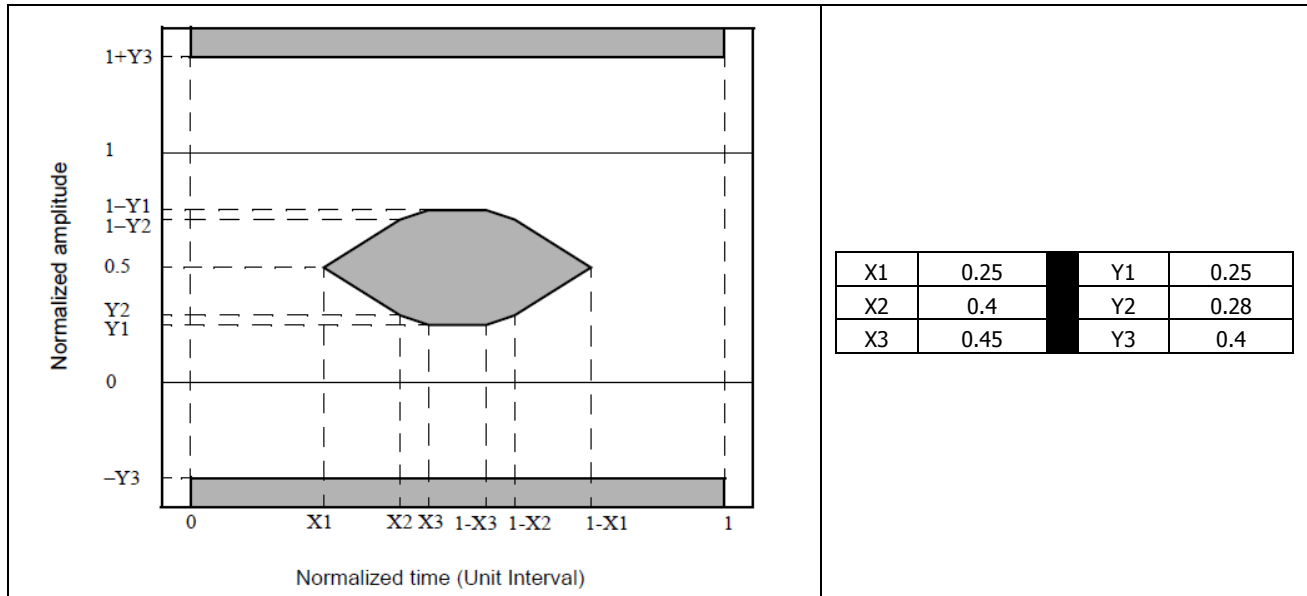


Optical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transmitter						
Lane wavelengths (Range)	λ_c	--	1264.5	1271	1277.5	nm
			1284.5	1291	1297.5	nm
			1304.5	1311	1317.5	nm
			1324.5	1331	1337.5	nm
Side Mode Suppression Ratio	SMSR	--	30	--	--	dB
Total average launch power	P _{tot}	--	--	--	8.3	dBm
Average launch power, each lane	P _o	--	-7	--	2.3	dBm
OMA, each lane	OMA	CW, ER>3.5dB	-4	--	3.5	dBm
Difference in launch power between any two lanes (OMA)	--	--	--	--	5	dB
Average launch power of OFF transmitter, each lane	P _{off}	--	--	--	-30	dBm
Extinction ratio	ER	--	3.5	--	--	dB
Eye mask definition	--	--	Compliance IEEE802.3ba			
Receiver						
Center Wavelength - lane 0	λ_{c0}	--	1264.5	--	1277.5	nm
Center Wavelength - lane 1	λ_{c1}	--	1284.5	--	1297.5	nm
Center Wavelength - lane 2	λ_{c2}	--	1304.5	--	1317.5	nm
Center Wavelength - lane 3	λ_{c3}	--	1324.5	--	1337.5	nm
Damage threshold	--	--	3.3	--	--	dBm
Receiver Power (OMA), each Lane	--	--	--	--	3.5	dBm
Receiver Reflectance	--	--	--	--	-26	dB
Difference in receiver power between any two lanes(OMA) (max)	--	--	--	--	7.5	dB
Average receive power, each lane	--	--	-13.7	--	2.3	dBm
Receiver sensitivity(OMA), each lane	R _{sens}	1	--	--	-11.5	dBm
Stress receiver sensitivity (OMA), each lane	--	2	--	--	-9.6	dBm
Rx LOS Assert	P _A	--	-28	--	--	dBm
Rx LOS De-Assert	P _D	--	--	--	-14	dBm
Rx LOS Hysteresis	P _A -P _D	--	0.5	--	--	dB

1. asured with PRBS 2³¹ -1 at 10⁻¹² BER, NRZ.
2. Conditions of stressed receiver sensitivity test:

Eye Mask Definition



Pin Descriptions

38	GND
37	TX1n
36	TX1p
35	GND
34	TX3n
33	TX3p
32	GND
31	LPMode
30	Vcc1
29	VccTx
28	IntL
27	ModPrsL
26	GND
25	RX4p
24	Rx4n
23	GND
22	RX2p
21	RX2n
20	GND

Top Side
Viewed From Top

Module Card Edge

GND	1
TX2n	2
TX2p	3
GND	4
TX4n	5
TX4p	6
GND	7
ModselL	8
ResetL	9
VccRx	10
SCL	11
SDA	12
GND	13
RX3p	14
Rx3n	15
GND	16
RX1p	17
RX1n	18
GND	19

Bottom Side
Viewed From Bottom

Pin Definition

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTTL-I	ModSelL	Module Select	
9	LVTTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVC MOS I / O	SCL	2-wire serial interface clock	
12	LVC MOS I / O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTTL-O	ModPrsL	Module Present	
28	LVTTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note 1 :

GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2 :

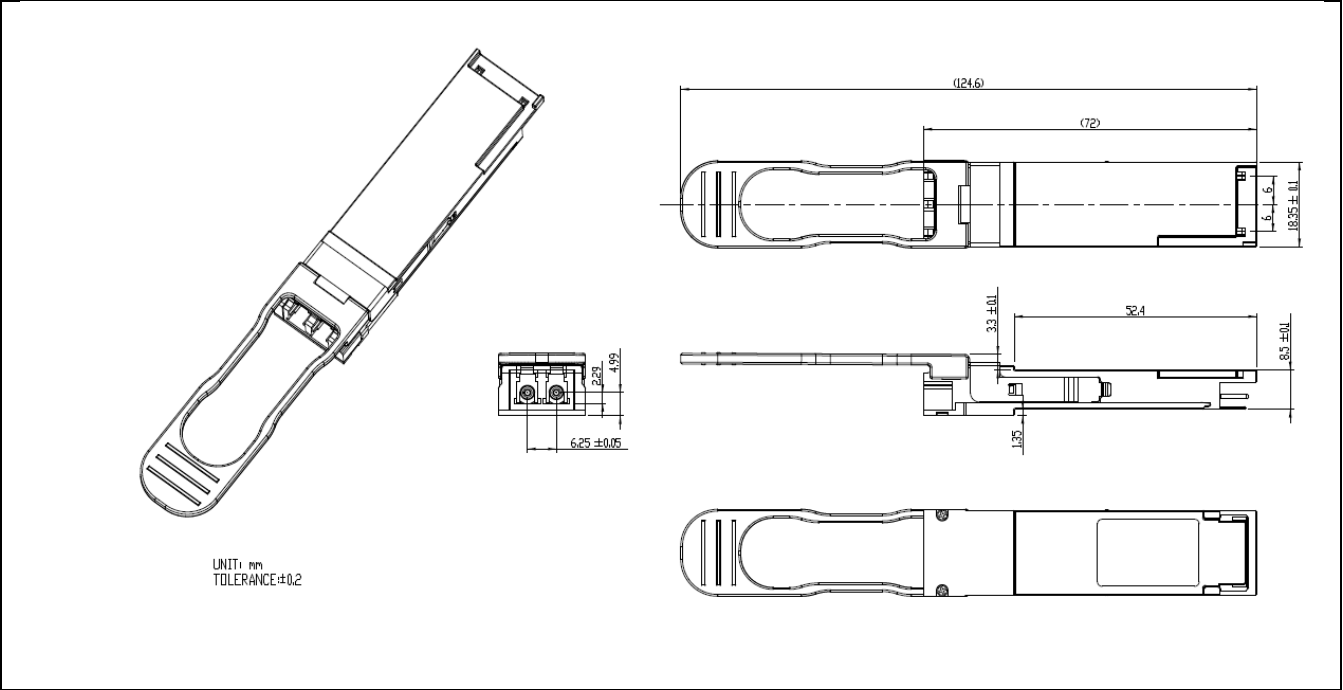
Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.



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Mechanical Design Diagram (mm)



Regulatory Compliance

Item	Standard
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B
Electrostatic Discharge to the Electrical Pins (ESD)	MIL-STD-883E Method 3015.7
Electrostatic Discharge to the Receptacle (ESD)	IEC 61000-4-2
RoHS	2011/65/EU
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11
Component Recognition	UL and TUV

Laser Safety Information

All versions of this laser are Class 1 laser products per IEC1/EN2 60825-1. Users should observe safety precautions such as those recommended by ANSI³ Z136.1, ANSI Z36.2 and IEC 60825-1.

This product conforms to FDA (CDRH) 21 CFR 1040.10 and 1040.11 except for deviations of laser safety class designation pursuant to '[Laser Notice No.50](#)'

Product labeling:

Class 1 Laser Product
Compliance with 21 CFR
1040.10 and 1040.11

If labeling is not affixed to the module due to size constraints; then rather, labeling is placed on the outside of the shipping box.

This product is not shipped with a power supply.

Caution: use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Certifications

UL	60950-1 (E243407)
TUV	EN60950-1, EN 60825-1, EN 60825-2

Documentation is available upon request.

(1) IEC is a registered trademark of the International Electrotechnical Commission

(2) Within Europe the IEC standard has been adopted as a European Normative standard known as EN 60825, and each European country will have its own version of this standard, for example, the British Standards version known as BS EN 60825. There can be small differences between the different countries versions of EN 60825, and these are in part caused by the process of translating the standard into the native language of that country.

(3) ANSI is a registered trademark of the American National Standards Institute

Note : All information contained in this document is subject to change without notice.